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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/644,215
Filing Date: August 20, 2003
Appellant(s): EMMOT ET AL.

EMMOT ET AL.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/08/2006 appealing from the Office action mailed 01/12/2006

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. 6,801,202	NELSON	10-2004
U.S. 6,311,247	SPENCER	10-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") in view of Spencer (6,311,247).

Nelson teaches a computer system (Figs. 2 and 3) comprising a host processor (102) configured to execute a single-threaded application; partitioning logic (such as, control unit 140 for dividing the stream of data received from computer system 80 into a corresponding number of parallel stream, col. 9, lines 20-24; and Fig. 22) for partitioning the state-sequenced information, communication logic (not shown, but can be any bus connectivity logic, such as, crossbar, chipset or bridge, see col. 8, lines 13-20, such as, arbiter in control unit of Fig. 22) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (shows one bus, but could be multiple separate busses since Nelson suggests one or more graphics processor 90, see col. 9, line 1, further see Spencer for the teachings of multiple busses); a plurality of interfaces (bus arbiter) located at a subsystem (112) for receiving the information communicated across the plurality of I/O busses; processing logic (graphics processor 90 in Fig. 3) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. However, Nelson fails to explicitly teach a plurality of I/O busses. This is what

Spencer teaches. Spencer teaches a computer system (Fig. 2) comprising a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information, communication logic (chipset 120) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (PCI buses 116-118); a plurality of interfaces (124-128) located at a subsystem for receiving the information communicated across the plurality of I/O busses; processing logic (not shown, but would have been obvious to connect any peripheral (I/O) devices into the PCI busses 116-118, for example, graphics processor is considered one of the peripheral device) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of separate multiple I/O or PCI busses into the system of Nelson in order to replace the single bus system of Nelson by the multiple busses of Spencer because multiple separate busses allows exclusive communication by providing a direct pipe therebetween and thus provides significant performance enhancements over prior art systems that have shared PCI busses as taught by Spencer (abstract). Therefore, at least claims 7, 9, 10, 12 and 14 would have been obvious.

As per claim 8, Spencer teaches a buffer memory (Fig. 4, cache 150) in communication with the host processor for storing state-sequenced information for communication to a subsystem.

As per claim 11, Spencer teaches the partitioning logic is located in at the host processor (Fig. 2, chipset 120).

As per claim 13, Nelson teaches the processing logic comprises at least one geometry accelerator (112).

As per claim 15, the combined system teaches the system comprises a plurality of processing nodes that are coupled through a communication network (Nelson, one or more graphics processor, col. 9, line 1 and Spencer, PCI devices connect into the PCI busses 116-118).

Method claims 1, 2 and 4-6 are similar in scope to system claims 7-15 above, and thus are rejected under similar rationale.

As per claim 3, Nelson teaches the communicating partitioned state-sequenced information comprises performing at least one DMA across each of the plurality of I/O busses (col. 8, lines 26-31).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") and Spencer (6,311,247) as applied to claims 7 and 15 above, and further in view of Ebihara et al (6,924,807 hereinafter "Ebihara").

The teachings of Nelson and Spencer are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach the processing logic comprises work queues maintained among the processing nodes. This is what Ebihara teaches. Ebihara teaches an image processing apparatus comprising a plurality of graphics processors (104), each being operable to render the image data (110) and at least one merge unit (106) operable to synchronously (108 or 118) receive the image data and synchronously (108 or 118) produce combined frame image data based thereon (abstract, Fig. 3). The Synchronous unit (108) performs similar functions as the work queue which provides synchronization among plurality of

graphics processor. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the synchron unit (108 or 118) into the combined system in order to provide synchronization among multiple graphics processors and thus to provide synchronized output signals. Therefore, at least claim 16 would have been obvious.

(10) Response to Arguments

Regarding 35 USC 103 rejections, Appellant argues "there is no teaching in Spencer of the host processor being configured to execute a single-threaded application." It is noted that even though Spencer is silent on whether the application being executed on the host processor is a single-threaded or multi-threaded application, it would have been obvious to one of ordinary skill in the art to implement Spencer because both single-threaded or multi-threaded provides advantages and for example, multi-threaded improves responsiveness, fast application and prioritization compares to single-threaded and single-threaded is slower and results in system idle time and user frustration. It is also noted that the examiner does not rely solely on Spencer reference since Nelson does teach single-threaded applications, and the host CPU providing the partitioned data to the graphics subsystem. Therefore, it would have been obvious in view of the combination of teachings of both Spencer and Nelson because both the computer system receive information from host computer and process the data based on the information (data and command) received from the host computer.

Appellant further argues that Spencer fails to teach the "partitioning logic". The examiner disagrees. Spencer clearly suggest that "I/O controller 123 generally operates to parse and reformat the signals carried on bus 125 into much smaller units that may be communicated

over a high-speed bus comprising much fewer conductors." (col. 5, lines 15-19). Furthermore, Nelson teaches the controller 140 may also divide the stream of data received from computer system 80 into a corresponding number of parallel streams that are routed to the individual rendering units 150A-D (col. 9, lines 20-24).

Appellant also argues that Spencer fails to teach the claimed "processing logic" and each of the PCI devices of Spencer performs its operations independently of the other PCI devices and therefore would have no reason or need to re-sequence any state-sequenced information because information sent to a disc driver controller (one of the PCI devices), would not be linked, in a state-sequenced fashion, with information sent to devices like video cards. The examiner agrees. However, the information sent to one of the video cards (one of the PCI devices), would be linked, in a state-sequenced fashion, with information sent to other video cards. It is noted that there are more than one video cards. Also, Nelson teaches processing logic (rendering units 150A-D and sample-to-pixel calculation unit 170A-D).

Nelson also teaches that the graphic subsystem 112 connected to the system bus 104 may comprise more than one graphics processor 90 (col. 8 line 67 to col. 9, line 1), and also the graphics processor 90 comprises more than one control unit 140 (col. 9, lines 10-12). Nelson also teaches the graphics system 112 may be coupled to more than one buses (col. 8, lines 11-23). Thus, with this configuration in accordance with Figs. 1-3, the graphics subsystem is not interfaced with the host system via a "*single* high-speed bus" as mischaracterized by Appellant, but in fact, via multiple I/O buses. Since Nelson also suggests that the graphics subsystem, which may include multiple graphics processors as cited above, can be configured to couple to different types of buses (col. 8, lines 11-20), these multiple graphics processors can interface with the

system bus 104 via multiple PCI interfaces, which is why the examiner relies on the secondary reference Spencer.

Then, Appellant argues that claim 2 further requires "obtaining state information from the received information, and processing the information in a proper state context" which would have been obvious in view of the teachings of processing logic of Spencer and Nelson because both the processing logic receiving information from host computer and processing the data based on the information (data and command) received from the host computer.

It is noted that Appellant argues the non-obviousness by attacking references individually where, as here the rejections are based on combination of references. *In re Keller*, 208 USPQ 871 (CCPA 1981).

In response to Appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the examiner clearly provided proper motivations to combine the multiple I/O busses of Spencer into the single I/O bus of Nelson as recited in the detail rejections above. Furthermore, Spencer clearly teaches the motivation to replace a shared single bus by multiple individual busses in order to provide significant performance enhancements over the prior art systems that have shared PCI buses - multiple PCI devices per PCI bus (see abstract).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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